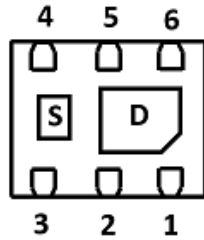
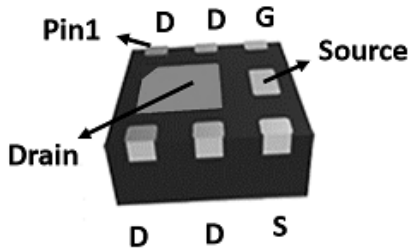
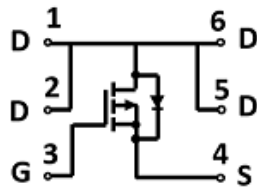


P-Channel Enhancement Mode Field Effect Transistor



DFN2x2-6L



Product Summary

• V_{DS}	-20V
• I_D	-7A
• $R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	<36.5mohm
• $R_{DS(ON)}$ (at $V_{GS}=-2.5V$)	<46.5mohm
• $R_{DS(ON)}$ (at $V_{GS}=-1.8V$)	<60.5mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-20	V
Gate-source Voltage	V_{GS}	± 10	V
Drain Current	I_D	$T_C=25^\circ C$ @ Steady State	-7
		$T_C=70^\circ C$ @ Steady State	-5.6
Pulsed Drain Current ^A	I_{DM}	-28	A
Total Power Dissipation @ $T_C=25^\circ C$ ^C	P_D	2.2	W
Thermal Resistance Junction-to-Ambient @ Steady State ^D	$R_{\theta JA}$	57	$^\circ C/W$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ4666B	F1	..G66B	3000	30000	120000	7 " reel



YJQ4666B

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-7A		24.5	36.5	mΩ
		V _{GS} = -2.5V, I _D =-5A		33.5	46.5	
		V _{GS} = -1.8V, I _D =-2A		45.5	60.5	
Diode Forward Voltage	V _{SD}	I _S =-7A, V _{GS} =0V		-0.7	-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		852		pF
Output Capacitance	C _{oss}			127		
Reverse Transfer Capacitance	C _{rss}			109		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-9V, I _D =-7A		40.1		nC
Gate Source Charge	Q _{gs}			8.4		
Gate Drain Charge	Q _{gd}			8.6		
Reverse Recovery Charge	Q _{rr}	I _F = -15A, di/dt=100A/us		7.8		
Reverse Recovery Time	t _{rr}			18		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-4.5V, V _{DD} =-9V, I _D =-1A, R _{GEN} =2.5Ω		8		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			75		
Turn-off Fall Time	t _f			46		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

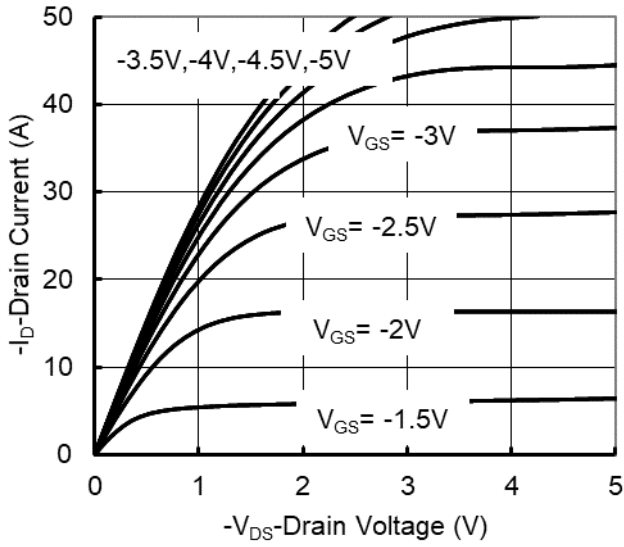


Figure 1. Output Characteristics

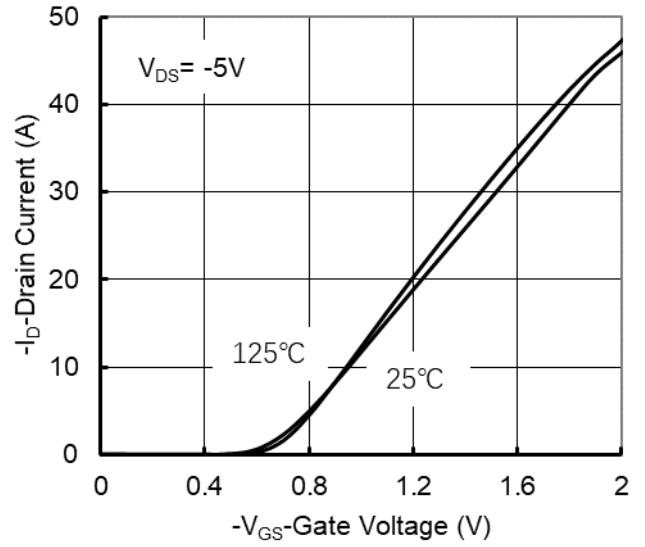


Figure 2. Transfer Characteristics

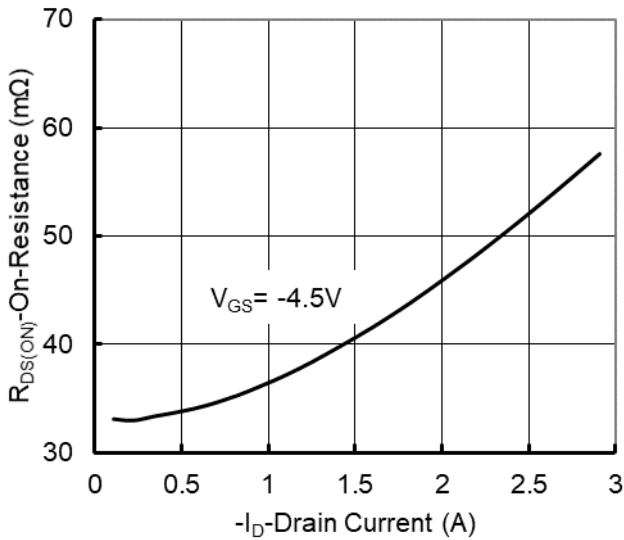


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

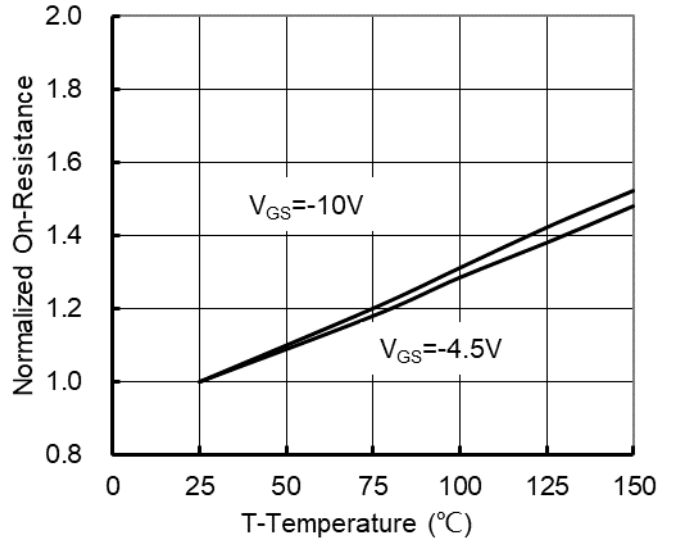


Figure 4. On-Resistance vs. Junction Temperature

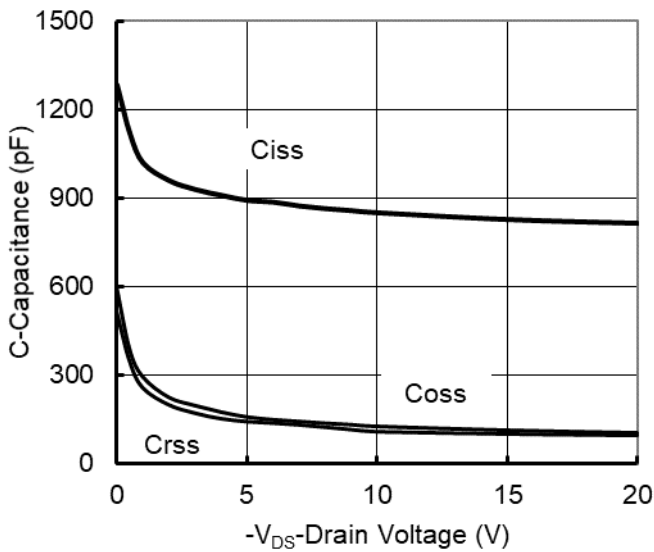


Figure 5. Capacitance Characteristics

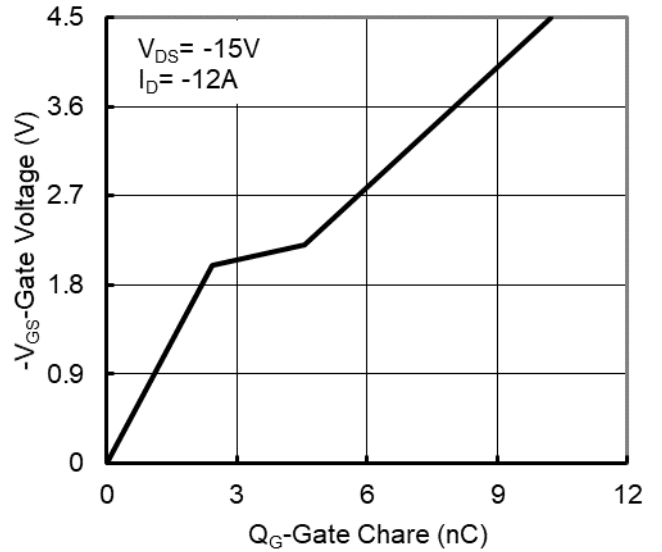


Figure 6. Gate Charge

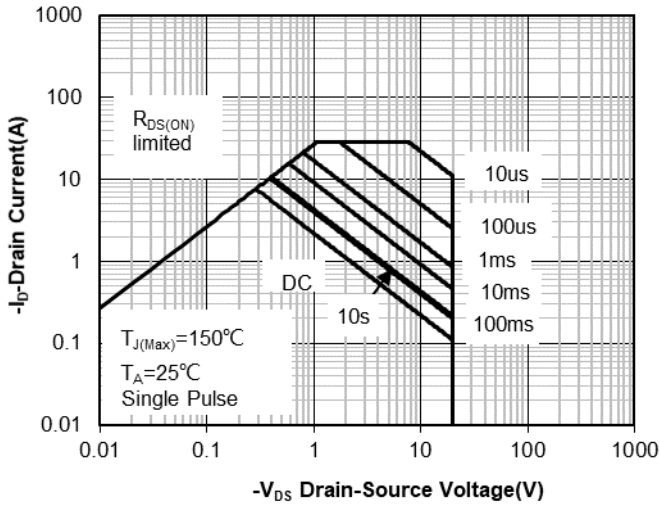


Figure 7. Safe Operation Area

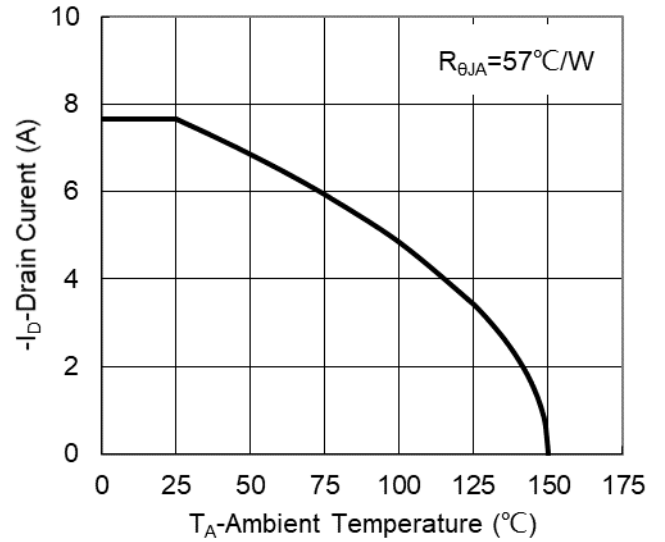


Figure 8. Maximum Continuous Drain Current vs Case Temperature

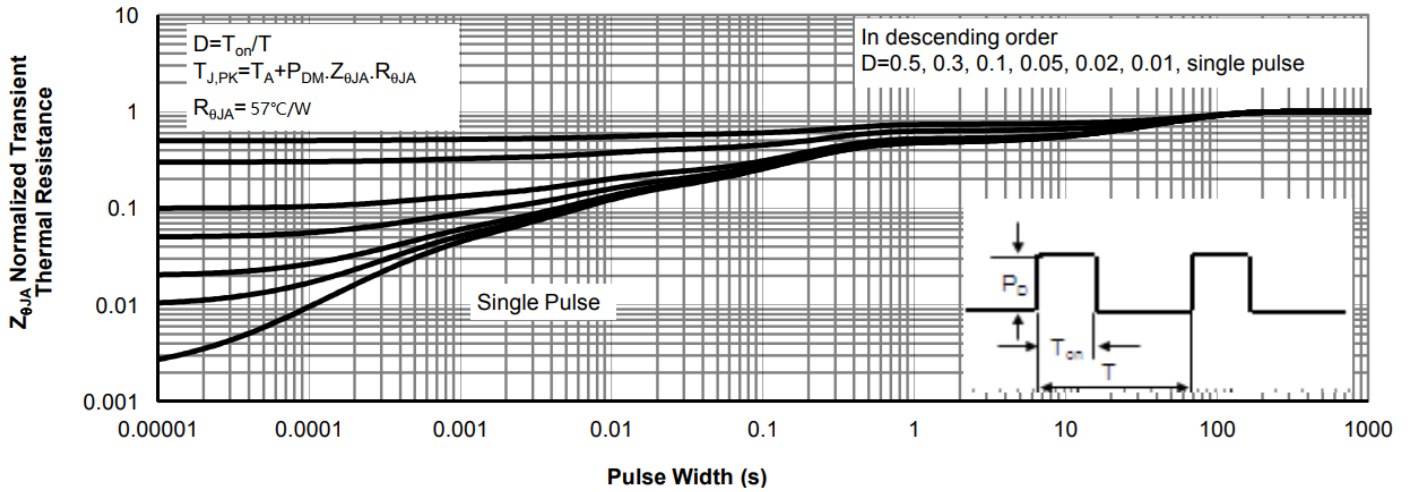
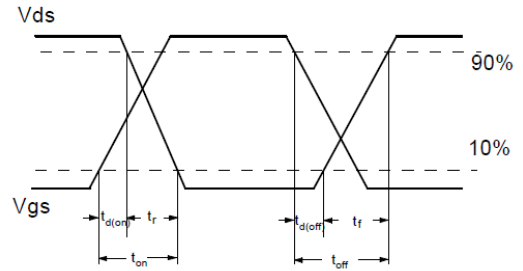
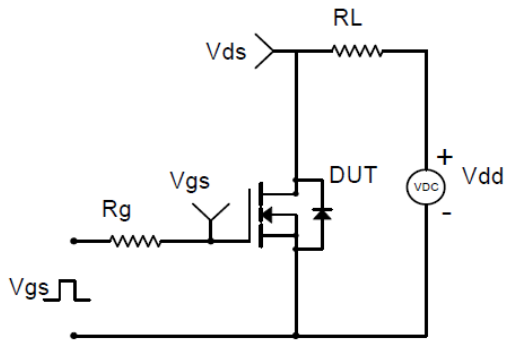
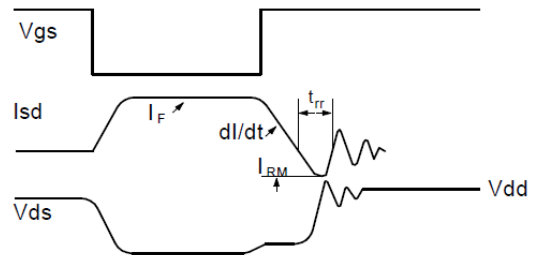
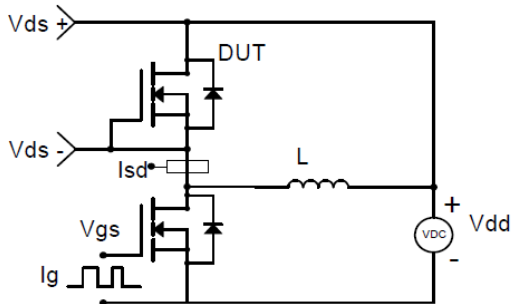


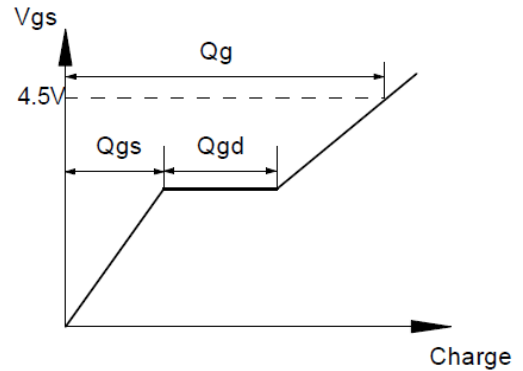
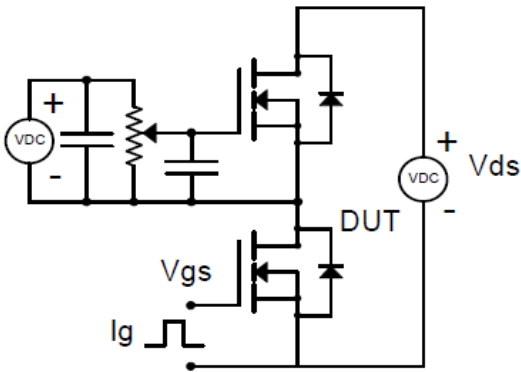
Figure 9. Normalized Maximum Transient Thermal Impedance



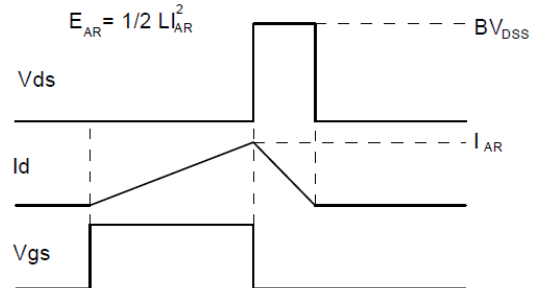
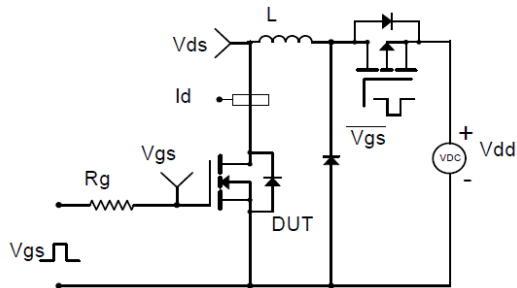
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

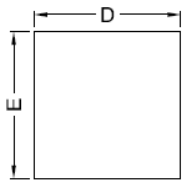


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

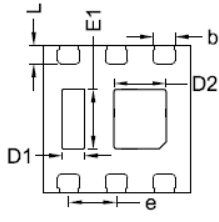


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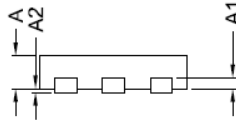
■ DFN2x2-6L(0.45mm) Package Information



Top View
正面视图



Bottom View
背面视图

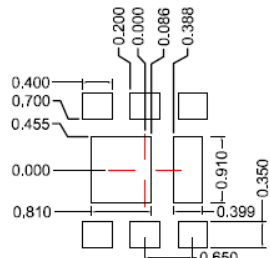


Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.35	0.45	0.55
A1	0.15 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View



YJQ4666B

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