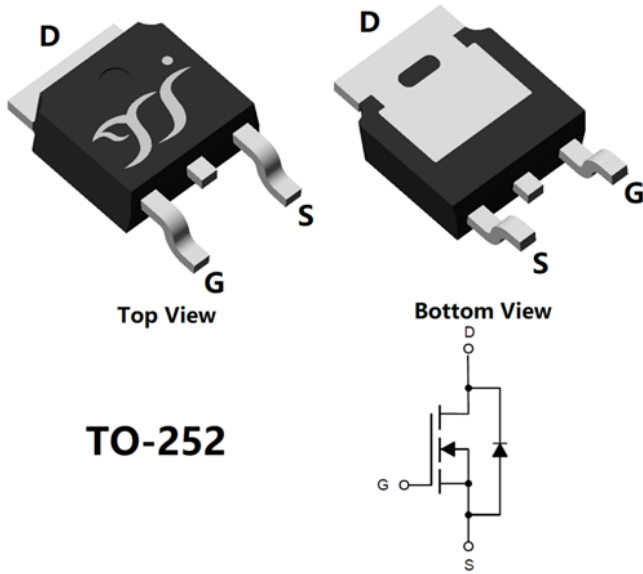


N-Channel Enhancement Mode Field Effect Transistor



TO-252

Product Summary

- V_{DS} 650V
- I_D 11A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<400m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Super Junction High Voltage MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Switching Mode Power Supplies (SMPS)
- PWM Motor Controls
- LED Lighting
- Adapter

Limiting Values

Parameter	Conditions	Symbol	Min	Max	Unit	
Drain-source Voltage		V_{DS}	-	650	V	
Gate-source Voltage		V_{GS}	-30	30		
Continuous Drain Current (Note 1,2)	Steady-State	I_D	$T_A=25^\circ C, V_{GS}=10V$	-	1.6	A
			$T_A=100^\circ C, V_{GS}=10V$	-	1	
Continuous Drain Current (Note 1,3)	Steady-State		$T_C=25^\circ C, V_{GS}=10V, \text{Chip limitation}$	-	11	
			$T_C=100^\circ C, V_{GS}=10V$	-	7	
Pulsed Drain Current	$T_C=25^\circ C, t_p \leq 10\mu s$	I_{DM}	-	28		
Maximum Body-Diode Continuous Current	$T_C=25^\circ C$	I_S		11		
Maximum Body-Diode Pulsed Current	$T_C=25^\circ C, t_p \leq 10\mu s$	I_{SM}	-	28		
Avalanche Energy (non-repetitive)	$T_J=25^\circ C, V_G=10V, R_G=25\Omega, L=30mH, I_{AS}=3.5A$	EAS	-	183.75	mJ	
Total Power Dissipation (Note 1,2)	Steady-State	P_D	$T_A=25^\circ C$	-	2.6	W
			$T_A=100^\circ C$	-	1	
Total Power Dissipation (Note 1,3)	Steady-State		$T_C=25^\circ C$	-	125	
			$T_C=100^\circ C$	-	50	
MOSFET dv/dt Ruggedness	$V_{DS}=0 \dots 325V, R_G=0\Omega$	dv/dt	-	17.8	V/ns	
Reverse Diode dv/dt	$V_{DS}=0 \dots 325V, I_D \leq 4A, di/dt=200A/\mu s$	dv/dt	-	12.4		
Maximum Diode Commutation Speed	$V_{DS}=0 \dots 325V, I_D \leq 4A, R_G=0\Omega$	dif/dt	-	2930	A/ μs	
Junction and Storage Temperature Range		T_J, T_{STG}	-55	150	$^\circ C$	

Thermal Resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	-	48	$^\circ C/W$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	-	1	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD400C65BHJ	F2	YJD400C65BH	2500	/	25000	13" reel



YJD400C65BHJ

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A, T_j=25^\circ C$	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ C$	-	-	1	μA
		$V_{DS}=650V, V_{GS}=0V, T_j=150^\circ C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V, T_j=25^\circ C$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A, T_j=25^\circ C$	3.2	4	4.8	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5A, T_j=25^\circ C$	-	355	400	m Ω
		$V_{GS}=10V, I_D=5A, T_j=150^\circ C$	-	886	999	
Diode Forward Voltage	V_{SD}	$I_S=11A, V_{GS}=0V, T_j=25^\circ C$	-	0.89	1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^\circ C$	-	6	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=325V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$	-	800	-	pF
Output Capacitance	C_{oss}		-	20	-	
Reverse Transfer Capacitance	C_{rss}		-	1.2	-	
Effective Output capacitance, Energy Related	$C_{o(er)}$	$V_{DS}=0\dots 325V, V_{GS}=0V, f=1MHz, T_j=25^\circ C$	-	33.5	-	
Effective Output Capacitance, Time Related	$C_{o(tr)}$		-	166	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=325V, I_D=5A, T_j=25^\circ C$	-	18.8	-	nC
Gate-Source Charge	Q_{gs}		-	4.7	-	
Gate-Drain Charge	Q_{gd}		-	8.3	-	
Reverse Recovery Charge	Q_{rr}	$I_F=5A, di/dt=100A/\mu s, V_{GS}=0V, V_R=325V, T_j=25^\circ C$	-	1933	-	nC
Reverse Recovery Time	t_{rr}		-	203	-	ns
Peak Reverse Recovery Current	I_{rrm}		-	17.7	-	A
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=325V, I_D=5A, R_{GEN}=3\Omega, T_j=25^\circ C$	-	22	-	ns
Turn-on Rise Time	t_r		-	22	-	
Turn-off Delay Time	$t_{D(off)}$		-	25	-	
Turn-off Fall Time	t_f		-	29	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



YJD400C65BHJ

Typical Electrical and Thermal Characteristics Diagrams

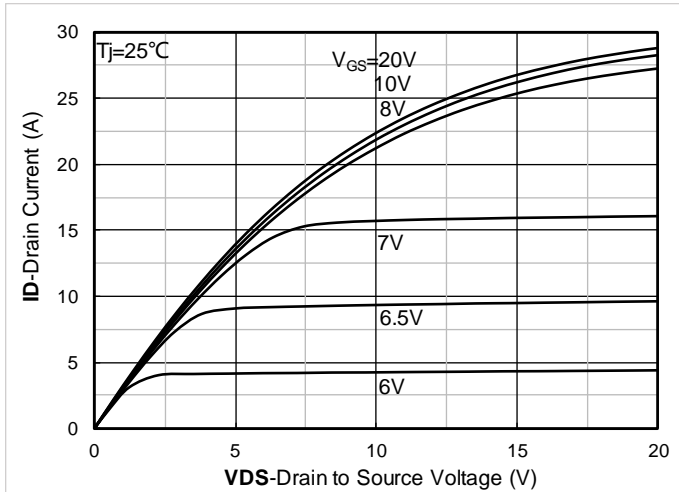


Figure 1. Output Characteristics; typical values

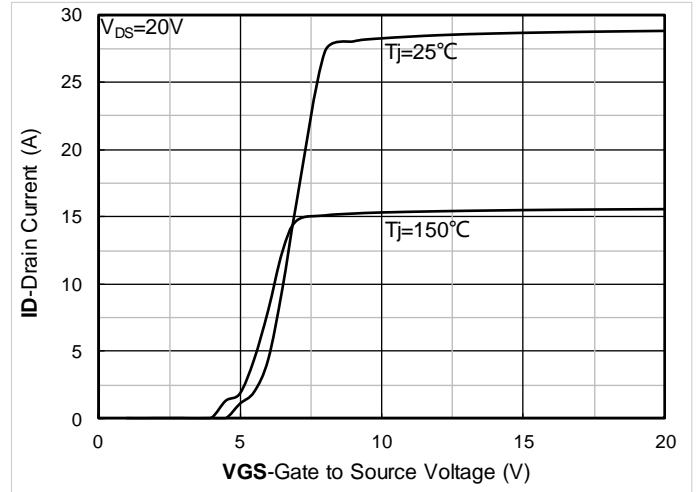


Figure 2. Transfer Characteristics; typical values

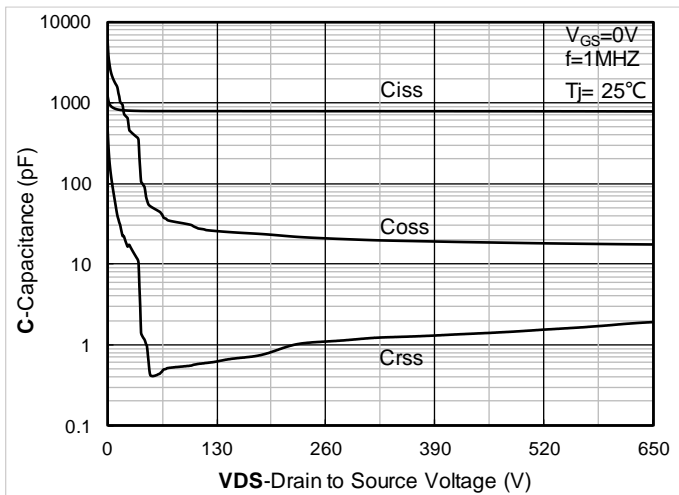


Figure 3. Capacitance Characteristics; typical values

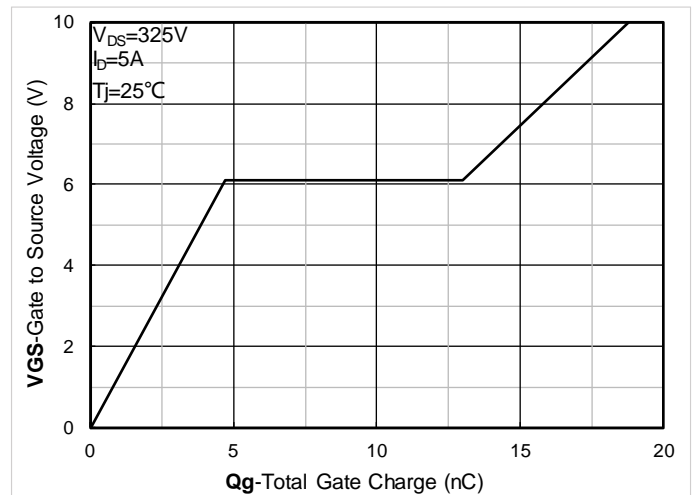


Figure 4. Gate Charge; typical values

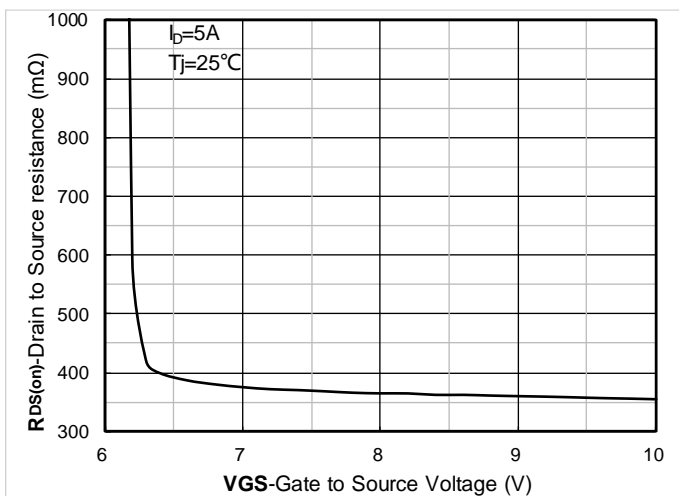


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

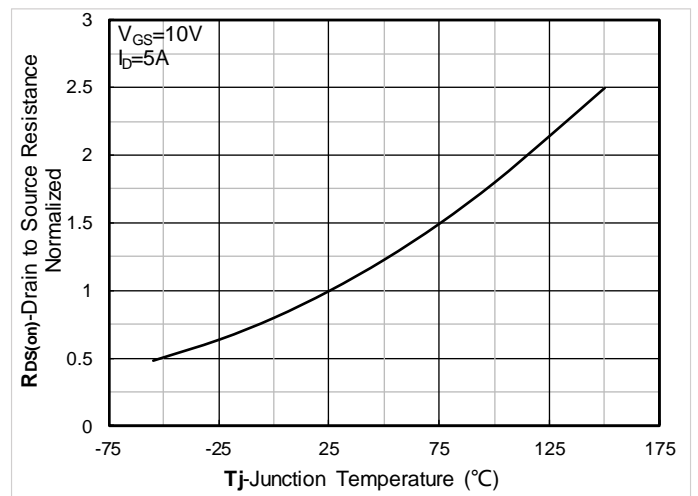


Figure 6. Normalized On-Resistance



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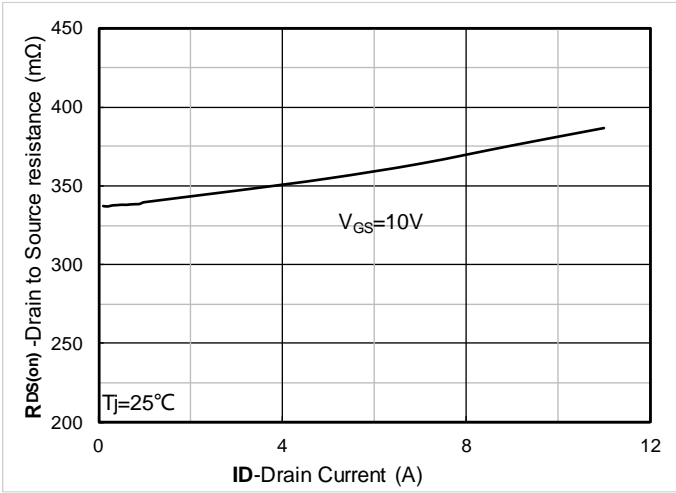


Figure 7. RDS(on) vs. Drain Current; typical values

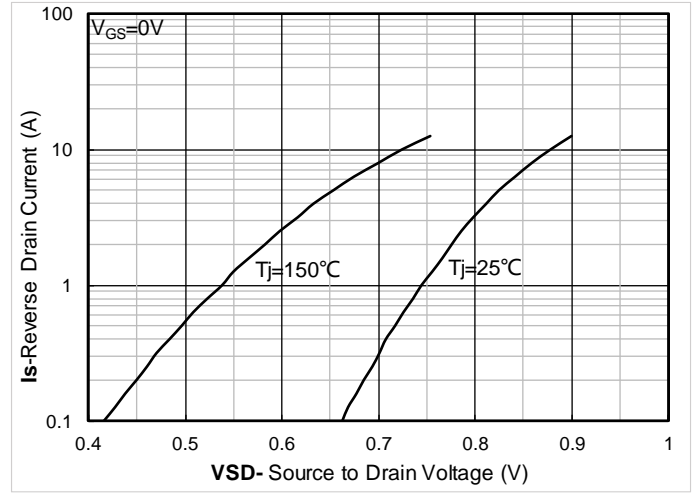


Figure 8. Forward characteristics of reverse diode; typical values

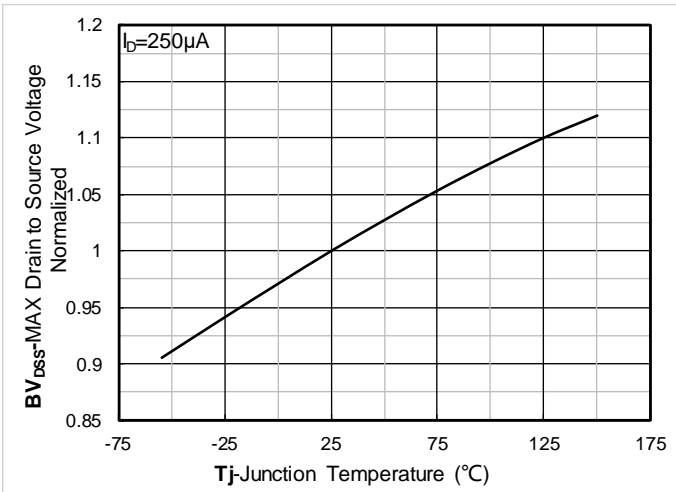


Figure 9. Normalized breakdown voltage

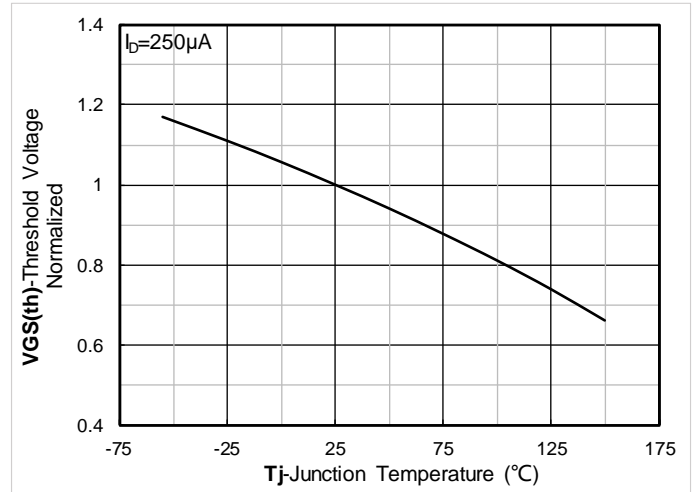


Figure 10. Normalized Threshold voltage

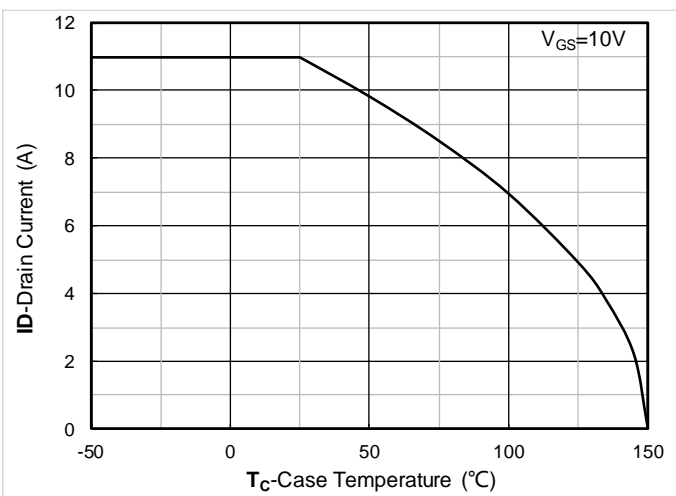


Figure 11. Current dissipation

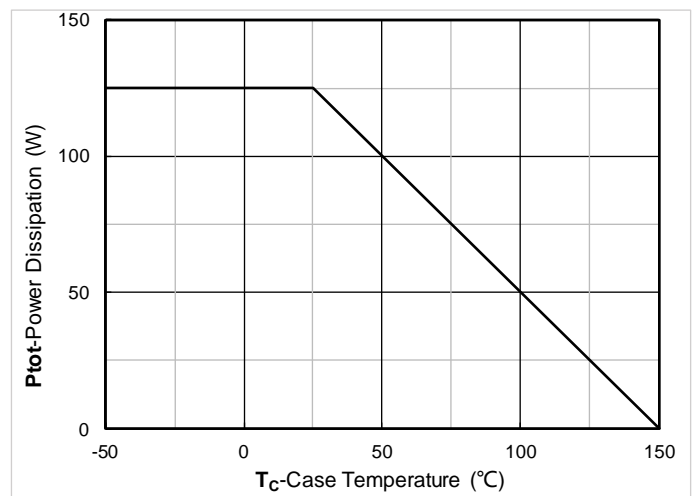


Figure 12. Power dissipation



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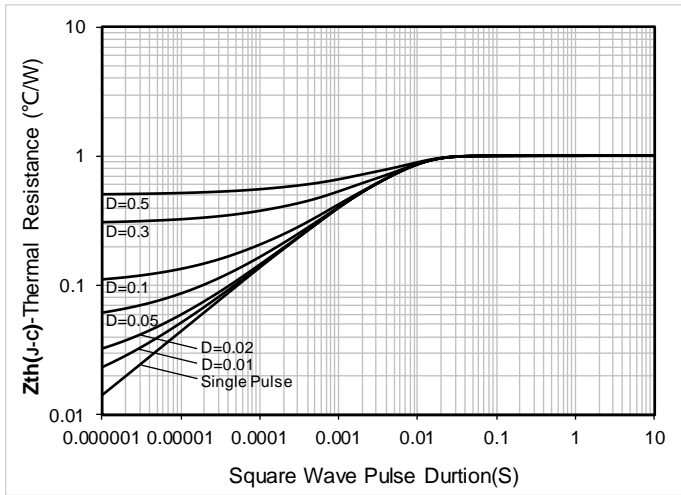


Figure 13. Maximum Transient Thermal Impedance

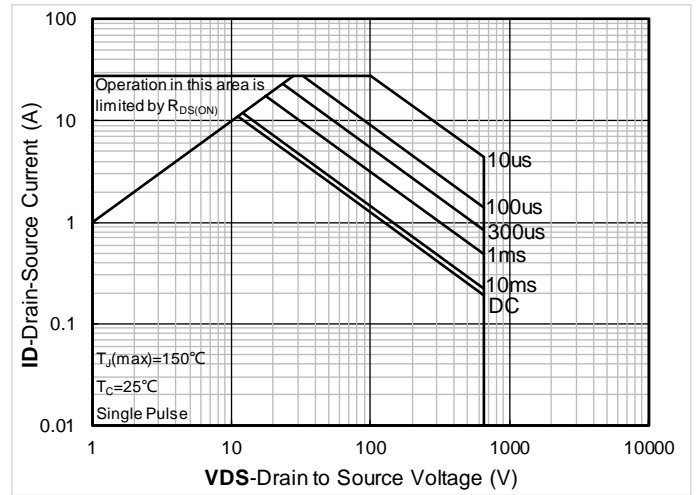


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

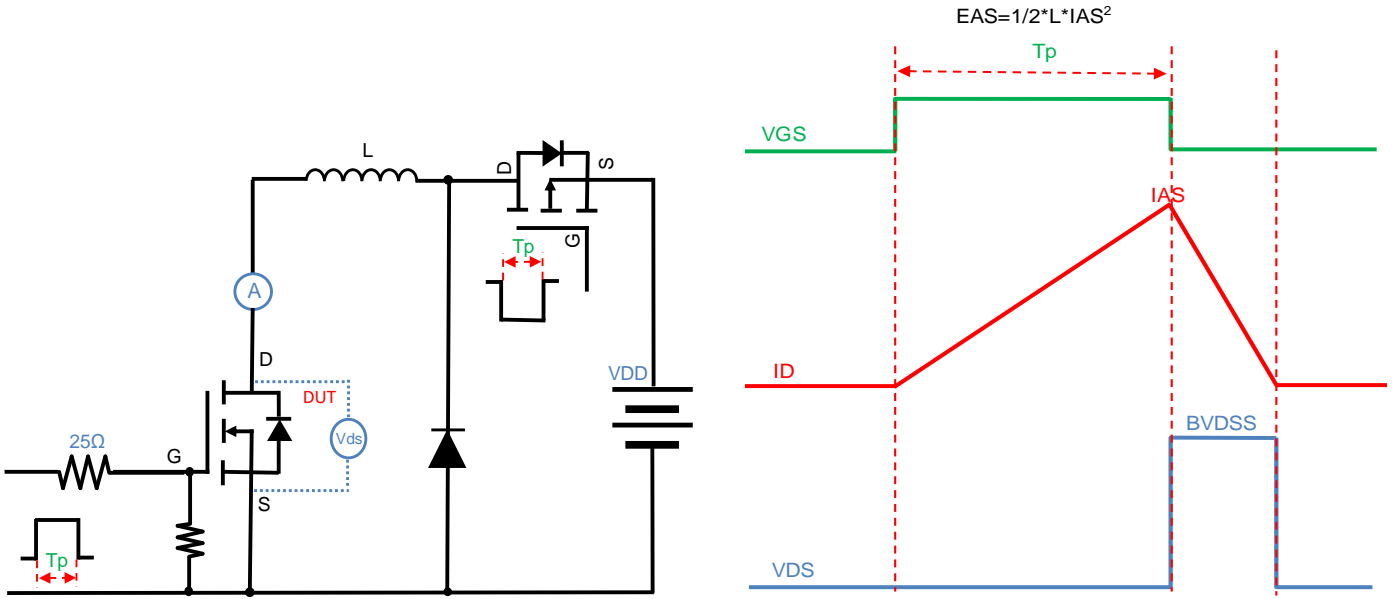


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

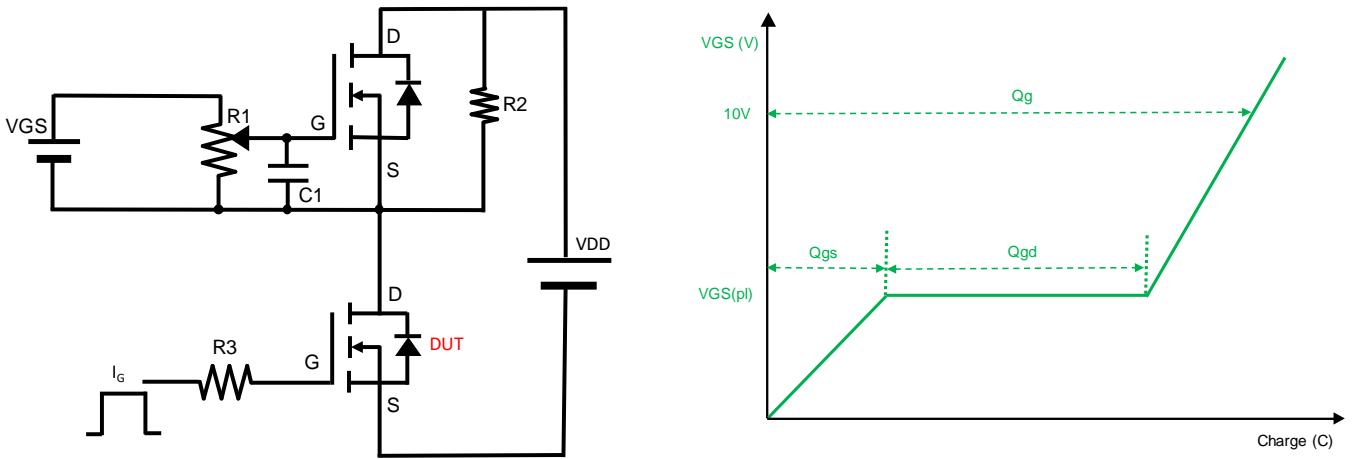


Figure B. Gate Charge Test Circuit & Waveform

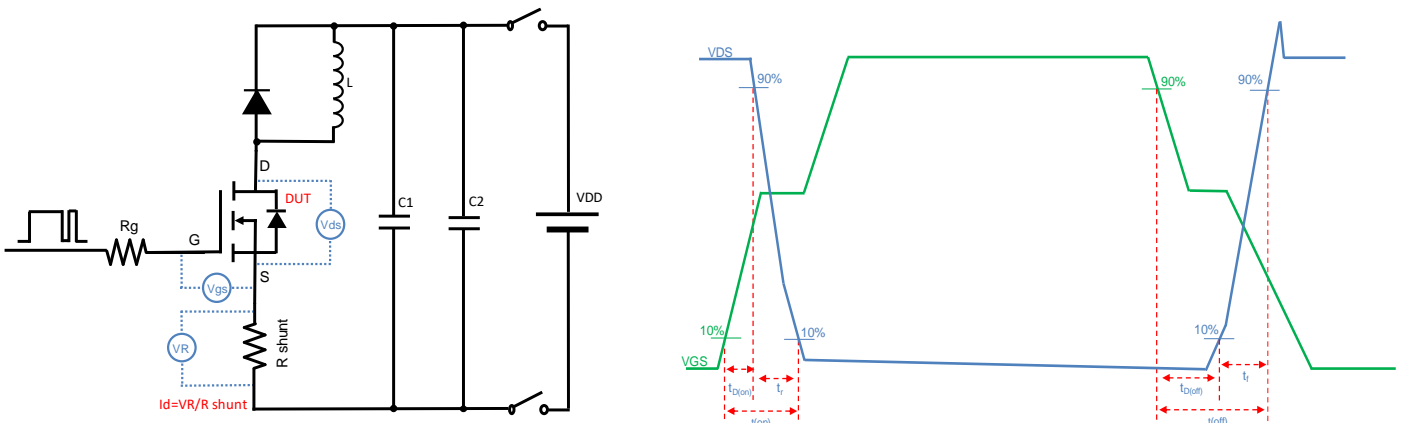


Figure C. Resistive Switching Test Circuit & Waveform

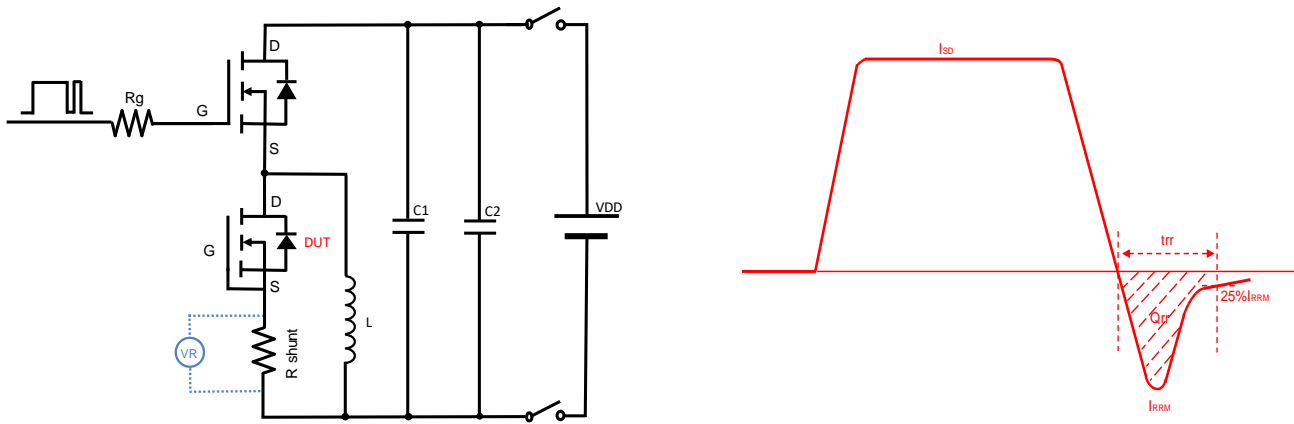
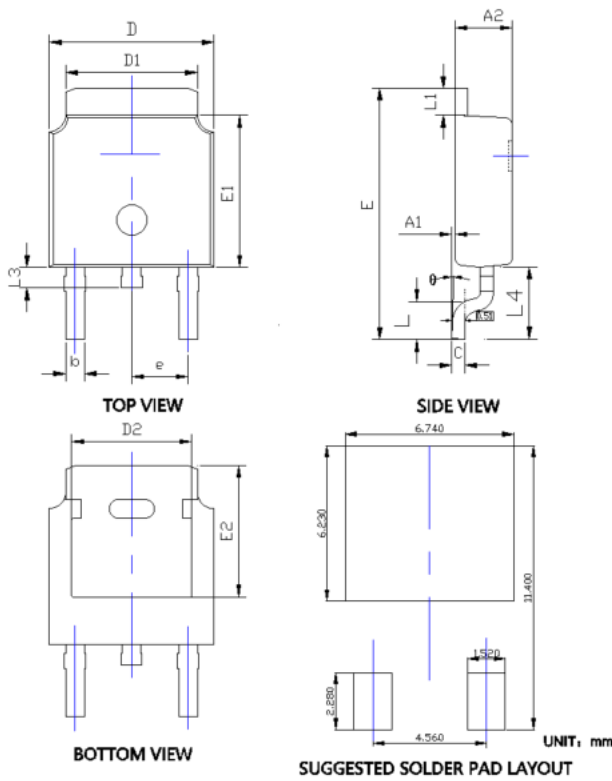


Figure D. Diode Recovery Test Circuit & Waveform



YJD400C65BHJ

■ TO-252-C Package information



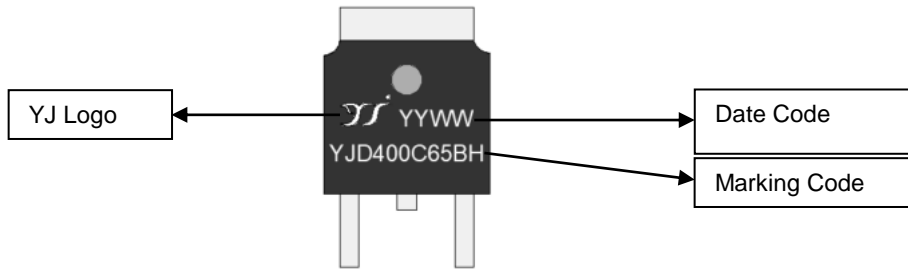
SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.000	0.008	0.000	0.200
A2	0.086	0.094	2.180	2.400
b	0.026	0.035	0.660	0.890
c	0.018	0.024	0.460	0.610
D	0.250	0.265	6.350	6.730
D1	0.195	0.215	4.950	5.460
D2	0.170	-	4.320	-
E	0.370	0.410	9.400	10.410
E1	0.235	0.245	5.970	6.220
E2	0.203	-	5.150	-
e	0.090	REF	2.286	REF
L	0.049	0.070	1.250	1.780
L1	0.035	0.050	0.890	1.270
L3	0.024	0.039	0.600	1.000
L4	0.102	0.126	2.600	3.200
θ	0°	10°	0°	10°

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



YJD400C65BHJ

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YJD400C65BH is marking code, YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



YJD400C65BHJ

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